



# FQP15P12/FQPF15P12

## 120V P-Channel MOSFET

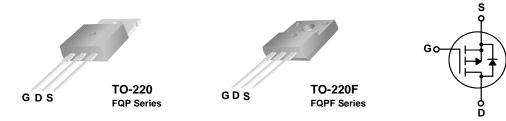
## **General Description**

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

#### **Features**

- -15A, -120V,  $R_{DS(on)}$  = 0.2 $\Omega$  @V<sub>GS</sub> = -10 V Low gate charge ( typical 29 nC)
- Low Crss (typical 110 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter		FQP15P12	FQPF15P12	Units
V <sub>DSS</sub>	Drain-Source Voltage		-120		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		-15	-15 *	Α
	- Continuous (T <sub>C</sub> = 100°C)	)	-10.6	-10.6 *	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	-60	-60 *	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		1157		mJ
I <sub>AR</sub>	Avalanche Current (No		-15		Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		10		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-5.0		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		100	41	W
	- Derate above 25°C		0.67	0.27	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +175		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

<sup>\*</sup> Drain current limited by maximum junction temperature.

## **Thermal Characteristics**

Symbol	Parameter	FQP15P12	FQPF15P12	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	3.66	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	40		°C/W
$R_{\theta JA}$	R <sub>θJA</sub> Thermal Resistance, Junction-to-Ambient		62.5	°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	-120			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to 25°C		-0.13		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -120 V, V <sub>GS</sub> = 0 V			-1	μΑ
		V <sub>DS</sub> = -96 V, T <sub>C</sub> = 150°C			-10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-2.0		-4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -7.5 \text{ A}$		0.17	0.2	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -40 \text{ V}, I_D = -7.5 \text{ A}$ (Note 4		9.5		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0  MHz		310 110	1100 400 140	pF pF
	,			110	140	Рі
t <sub>d(on)</sub>	Ing Characteristics Turn-On Delay Time			15	40	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = -60 \text{ V}, I_{D} = -15 \text{ A},$		100	210	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_G = 25 \Omega$		80	170	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4, 5		80	170	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -96 V, I <sub>D</sub> = -15 A,		29	38	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = -90 \text{ V}, I_D = -13 \text{ A},$ $V_{GS} = -10 \text{ V}$		5.1		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4, 5)		15		nC
<u> </u>	, ,	1			1	1
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-15	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F				-60	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -15 \text{ A}$			-4.0	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = -15 \text{ A},$		126		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$ (Note 4)		0.61		μС

- Notes: 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 6.0mH,  $I_{AS}$  = -15A,  $V_{DD}$  = -50V,  $R_G$  = 25  $\Omega$ , Starting  $T_J$  = 25°C 3.  $I_{SD} \le$  -15A,  $di/dt \le 300A/\mu_S$ ,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J$  = 25°C 4. Pulse Test : Pulse width  $\le 300\mu_S$ , Duty cycle  $\le 2\%$  5. Essentially independent of operating temperature

# **Typical Characteristics**

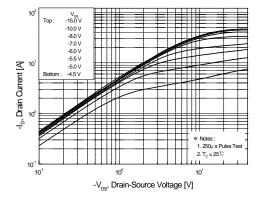


Figure 1. On-Region Characteristics

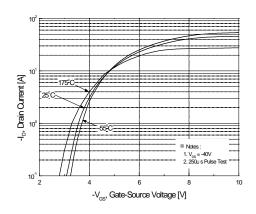


Figure 2. Transfer Characteristics

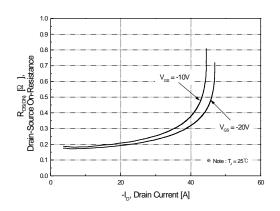


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

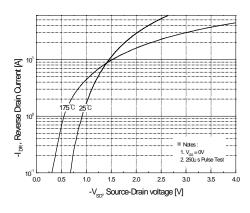


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

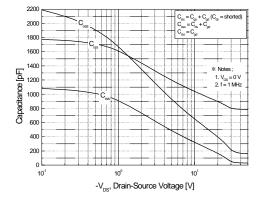


Figure 5. Capacitance Characteristics

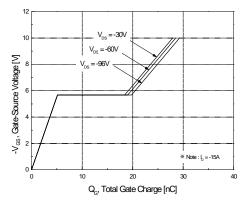


Figure 6. Gate Charge Characteristics

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# Typical Characteristics (Continued)

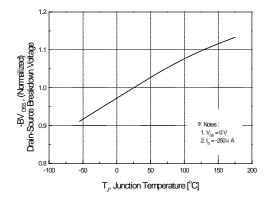


Figure 7. Breakdown Voltage Variation vs Temperature

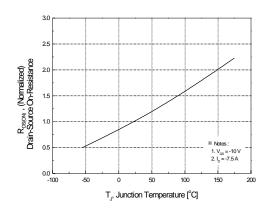


Figure 8. On-Resistance Variation vs Temperature

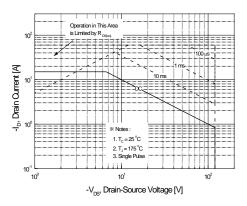


Figure 9-1. Maximum Safe Operating Area for FQP15P12

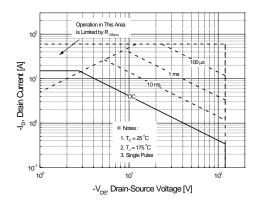


Figure 9-2. Maximum Safe Operating Area for FQPF15P12

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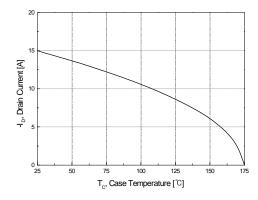


Figure 10. Maximum Drain Current vs Case Temperature

# Typical Characteristics (Continued)

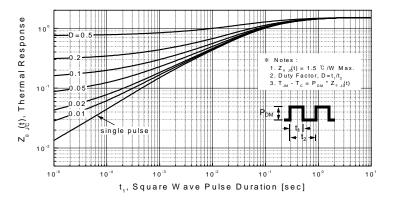


Figure 11-1. Transient Thermal Response Curve for FQP15P12

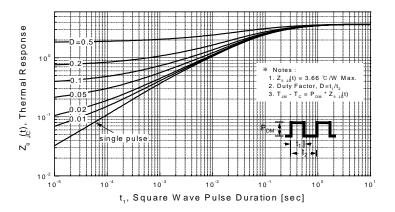
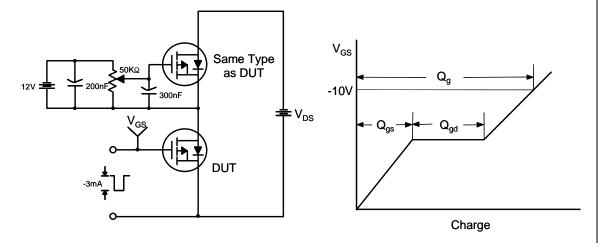
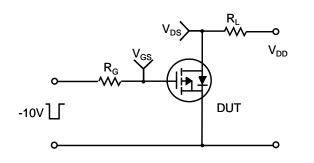


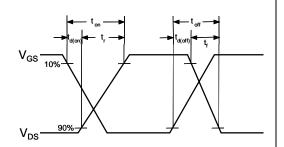
Figure 11-2. Transient Thermal Response Curve for FQPF15P12

## **Gate Charge Test Circuit & Waveform**

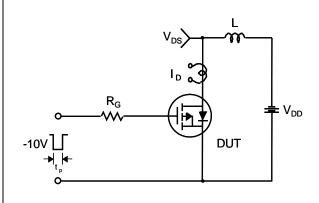


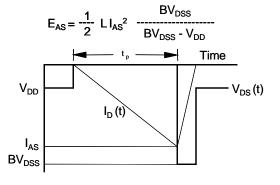
## **Resistive Switching Test Circuit & Waveforms**



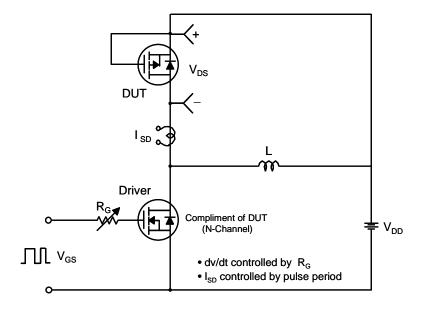


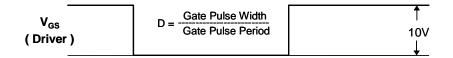
## **Unclamped Inductive Switching Test Circuit & Waveforms**

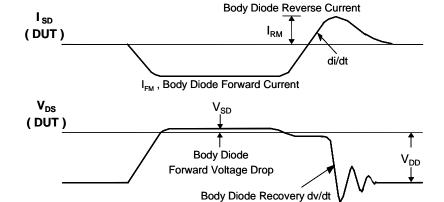


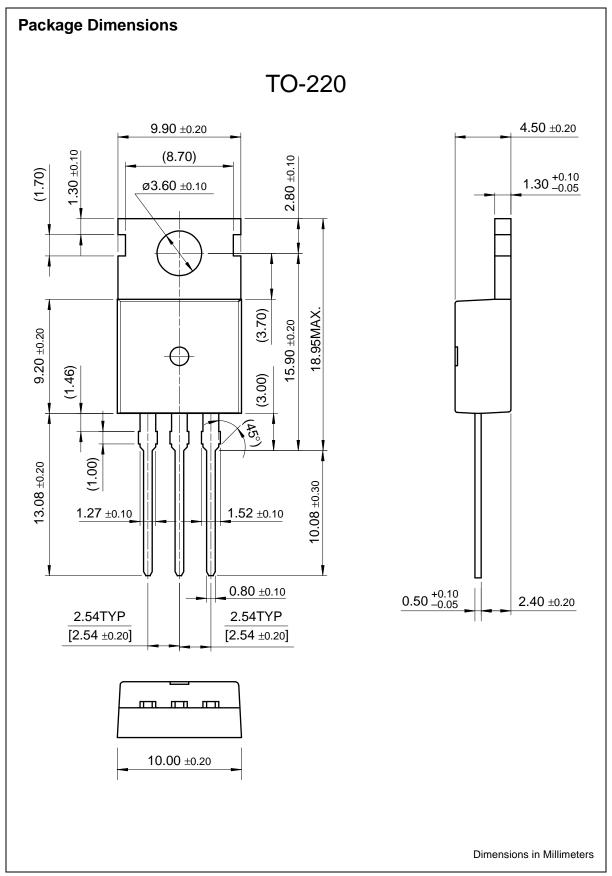


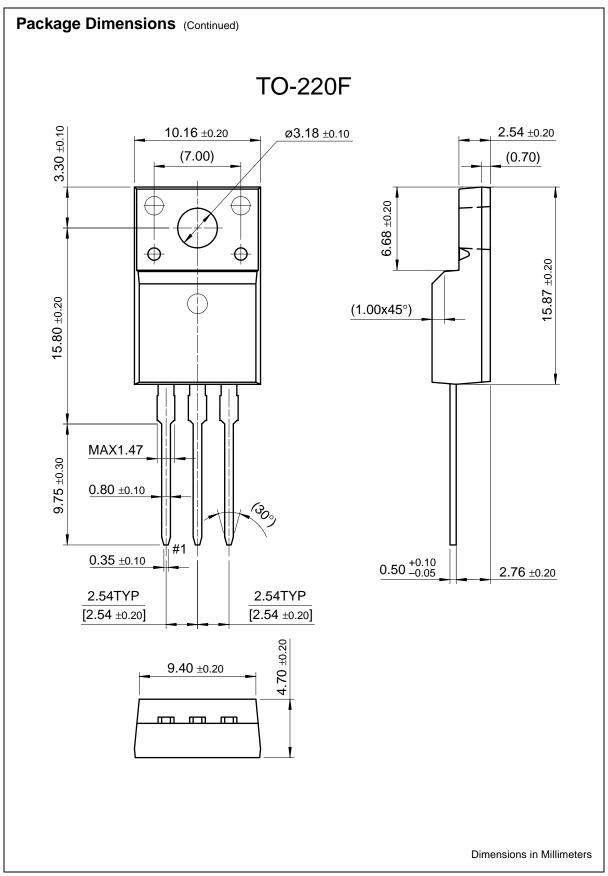
## Peak Diode Recovery dv/dt Test Circuit & Waveforms











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